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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/975,293	10/11/2001	Max M. Yeung	01-3221496.00144	1284

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EXAMINER	
TORRES, JOSEPH D	

ART UNIT	PAPER NUMBER
2133	3

DATE MAILED: 01/07/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/975,293	YEUNG ET AL.	
	Examiner	Art Unit	
	Joseph D. Torres	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 December 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 October 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. §§ 119 and 120

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

13)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application) since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

a) ☐ The translation of the foreign language provisional application has been received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121 since a specific reference was included in the first sentence of the specification or in an Application Data Sheet. 37 CFR 1.78.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *2*.
4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. New corrected drawings are required in this application because the handwriting in the drawings is difficult to read. Applicant is advised to employ the services of a competent patent draftsperson outside the Office, as the U.S. Patent and Trademark Office no longer prepares new drawings. The corrected drawings are required in reply to the Office action to avoid abandonment of the application. The requirement for corrected drawings will not be held in abeyance.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claims 1-20 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 1 recites the limitation "said syndrome signal" in line 7. There is insufficient antecedent basis for this limitation in the claim (Note: “said multi-bit syndrome signal” in lines 3 and 4 does not provide antecedent basis for the claim).

Claim 12 recites the limitation "said error location generation" in 5. There is insufficient antecedent basis for this limitation in the claim.

Claims 2-13 depend from claim 1, hence inherit the deficiencies of claim 1.

Claim 13 depends from claim 12, hence inherits the deficiencies of claim 12.

Claims 14 and 15 recite similar language as in claim 1.

Claims 16-20 depend from claim 15, hence inherit the deficiencies of claim 15.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

3. Claims 1-11 and 14-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Hsiao, Mu-Yue et al. (US 3623155 A, hereafter referred to as Hsiao) in view of Horiguchi, Masashi et al. (US 4726021 A, hereafter referred to as Horiguchi).

35 U.S.C. 103(a) rejection of claims 1, 14 and 15.

Hsiao teaches an apparatus for error control coding (see Figure 1 in Hsiao) comprising: a first circuit configured to generate a multi-bit digital syndrome signal in response to a

read data signal and a read parity signal (Figure 1 and col. 4, lines 23-30 in Hsiao teach that Error Detector Unit 5 in Figure 1 is a first circuit configured to generate an 8-bit multi-bit digital syndrome signal in response to 72 bits read from a communication path consisting of 64 bits of information and 8 bits of parity; hence Hsiao teaches a first circuit configured to generate an 8-bit multi-bit digital syndrome signal in response to a read data signal, 64 bits of information included in the 72 bits read from a communication path, and a read parity signal, 8 bits of parity included in the 72 bits read from a communication path); and a second circuit (combined OR-circuit 7, OR-circuit 8, AND-circuit 9, AND-circuit 10 and Error Locator Unit 11 in Figure 1 of Hsiao comprise a second circuit) configured to i. detect an error when said bits of said syndrome signal are not all the same state (col. 4, lines 34 of Hsiao teach that if any of the syndromes S1 to S8 is non-zero, i.e. not all the same zero state, an error signal is placed on an error line indicative of the error) and ii. generate an error location signal in response said syndrome signal (col. 11, lines 9-15 in Error Locator 11 in Hsiao teach that the Error Locator Unit 11 in Figure 1 which produces a 72-bit error indication error location signal for indicating the location of errors in response said syndrome signal [S1, S2, ..., S8]), wherein said error location signal is generated in response to fewer than all of said bits of said syndrome signal (Note: col. 2, lines 6-33 of Hsiao teach that an error location is determined by matching non-zero syndromes to columns in a table, hence only the non-zero syndromes are used to determine a location, e.g., if S1 and S2 are non-zero D0 is the erroneous bit, if S1 is non-zero C2 is the erroneous bit, if S2 and S3 are non-zero D1 is the erroneous bit, etc.; col. 3, lines 10-20 of Hsiao teach the use of an SEC/DED

(7,3)-code whereby said error location signal is always generated in response to fewer than all of said bits of said syndrome signal since to determine any single error in any 7-bit data stream, less than all of the syndromes need to be non-zero).

However Hsiao does not explicitly teach the specific use of **memory** error control coding.

The Examiner asserts that Hsiao teaches error control for a communications and processing systems (col. 1, lines 8-11 in Hsiao; Note: the Authoritative Dictionary of IEEE Standard Terms defines processing unit as a functional unit that consists of one or more processors and their storage), hence it would be obvious to use the error correction system taught in the Hsiao patent in an embodiment comprising a processing unit with memory since that is what the teachings in the Hsiao patent are explicitly designed for.

Horiguchi teaches a semiconductor memory circuit that is typically used in processing systems. In addition, Horiguchi teaches an error correction circuit 25 in Figure 1 of Horiguchi with a Syndrome Generator 111 and Error Location Indicator 112 connected to error correction circuitry, which are substantially the same in design as Figure 1 of Hsiao (Note: the EOR gates and the AND Gates for Switching Error correction on and off in Figure 11 in Horiguchi are substantially equivalent to or an embodiment of the Error Corrector circuit 13 in Hsiao, the Error Location Indicator 112 in Horiguchi is substantially equivalent to the Error Locator circuitry 11 in Hsiao and the Syndrome Generator 111 in Horiguchi is substantially equivalent to the Error Detector 5 in Hsiao). The difference being that Hsiao teaches the well-known and commonly-used use of

tables for matching syndromes to erred bits that Horiguchi fails to mention, that is, the internal functioning of the Error Location Indicator 112 in Horiguchi (Clearly the use of tables is an intended embodiment of the Horiguchi patent since the error correction circuitry in Horiguchi is designed to accommodate Hamming codes, which generally use tables for matching syndromes to erred bits). Hence, one of ordinary skill in the art at the time the invention was made would have had a more than reasonable expectation for success upon combining the Horiguchi patent and Hsiao patent, since the circuit design used in the two patents is substantially the same.

One of ordinary skill in the art at the time the invention was made would have been highly motivated to employ the error correction system taught in the Hsiao patent in an embodiment comprising a processing unit with memory, for which it was explicitly designed in order to reduce the complexity of the circuit design (col. 3, lines 3-10, Hsiao).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hsiao with the teachings in the Horiguchi patent by using the error correction system taught in the Hsiao patent in an embodiment comprising a processing unit with memory, for which it was explicitly designed. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that using the error correction system taught in the Hsiao patent in an embodiment comprising a processing unit with memory, for which it was explicitly designed would

have provided the opportunity to reduce the complexity of the circuit design (col. 3, lines 3-10, Hsiao).

35 U.S.C. 103(a) rejection of claim 2.

Col. 4, lines 34 of Hsiao teach that only if any of the syndromes S1 to S8 is non-zero, i.e. not all the same zero state, an error signal is placed on an error line indicative of the error, hence if all the syndrome bits are at the zero state, no error is detected.

35 U.S.C. 103(a) rejection of claims 3 and 19.

Note: col. 2, lines 6-33 of Hsiao teach that an error location is determined by matching non-zero syndromes to columns in a table, hence only the non-zero syndromes are used to determine a location, e.g., if S1 and S2 are non-zero D0 is the erroneous bit, if S1 is non-zero C2 is the erroneous bit, if S2 and S3 are non-zero D1 is the erroneous bit, etc.; hence if all the syndromes are zero no error is detected and the Error indication signal from the Error Locator circuit does not modify the correct data bits so that the original read data and parity signals are produced at an output of the Error Corrector 13 in Figure 1 of Hsiao.

35 U.S.C. 103(a) rejection of claim 4.

Hsiao and Horiguchi teach said apparatus comprises a memory circuit (see Figure 1 in Horiguchi) configured to i. receive a data input signal and a parity signal and ii. present

said read data and parity signals during a read operation (see Data Line Selector 21 in Figure 1 of Horiguchi).

35 U.S.C. 103(a) rejection of claims 5 and 18.

Hsiao and Horiguchi teach said second circuit is configured to generate i. a single error signal when a single bit error is detected in said read data and parity signals, ii. a double error signal when an error is detected in two bits of said read data and parity signals (the Abstract in Hsiao teaches that the error correction code is an SEC/DED code), and iii. an error detected signal when either said single error signal or said double error signal are generated in response to said syndrome signal (see Error line in Figure 1 of Hsiao).

35 U.S.C. 103(a) rejection of claims 6 and 20.

See Error Corrector 13 in Figure 1 of Hsiao.

35 U.S.C. 103(a) rejection of claim 7.

See inverters 16-23 in Figure 4 of Hsiao.

35 U.S.C. 103(a) rejection of claim 8.

Hsiao and Horiguchi, substantially teaches the claimed invention described in claims 1-7 (as rejected above).

However Hsiao and Horiguchi do not explicitly teach the specific use of specific circuitry for implementing the binary operations required by the parity generators taught in the Hsiao and Horiguchi patents.

The Examiner asserts that Hsiao teaches the use of Hamming codes (col. 6, lines 38-41, Hsiao) which is generated by mathematically applying a binary matrix to an input vector to perform a binary matrix multiplication. It would be obvious, to use a particular set of logic gates for the encoders in the Hsiao and Horiguchi patents to implement the required binary matrix multiplication used to produce parity based on obvious engineering design choices such as available circuitry, space requirements and operational speed requirements and since that is what binary logic gates are used for, to implement binary logic.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hsiao and Horiguchi by use of specific circuitry for implementing the binary operations required by the parity generators taught in the Hsiao and Horiguchi patents. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of specific circuitry for implementing the binary operations required by the parity generators taught in the Hsiao and Horiguchi patents would have provided the opportunity for implementing the binary operations required by the parity generators taught in the Hsiao and Horiguchi patents based on obvious engineering design choices such as available circuitry, space requirements and

operational speed requirements and since that is what binary logic gates are used for, to implement binary logic.

35 U.S.C. 103(a) rejection of claim 9.

Hsiao and Horiguchi, substantially teaches the claimed invention described in claims 1-8 (as rejected above). In addition, Hsiao and Horiguchi teach one or more OR gates configured to receive said syndrome signal and present said error detected signal (see OR gate 7 and Error line in Figure 1 of Hsiao); one or more AND gates configured to present said single error signal in response to said error detected signal and said intermediate signal (see AND gate 9 in Figure 1 of Hsiao); and an AND gate configured to present said double error signal in response to said error detected signal and an inverse of said intermediate signal (see AND gate 10 in Figure 1 of Hsiao).

However Hsiao and Horiguchi do not explicitly teach the specific use of one or more exclusive-OR gates configured to receive said syndrome signal and present an intermediate signal required by the error locators taught in the Hsiao and Horiguchi patents.

The Examiner asserts Hsiao and Horiguchi teach the use of tables to generate an intermediate error indicating value in Figure 1 from syndromes, which is mathematically equivalent to a binary matrix multiplication by a syndrome vector. It would be obvious, to use a particular set of logic gates for the error locators in the Hsiao and Horiguchi patents to implement the required binary matrix multiplication used to produce intermediate error indication values based on obvious engineering design choices such

as available circuitry, space requirements and operational speed requirements and since that is what binary logic gates are used for, to implement binary logic.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hsiao and Horiguchi by use of one or more exclusive-OR gates configured to receive said syndrome signal and present an intermediate signal required by the error locators taught in the Hsiao and Horiguchi patents. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of one or more exclusive-OR gates configured to receive said syndrome signal and present an intermediate signal required by the error locators taught in the Hsiao and Horiguchi patents would have provided the opportunity for implementing the binary operations required by the error locators taught in the Hsiao and Horiguchi patents based on obvious engineering design choices such as available circuitry, space requirements and operational speed requirements and since that is what binary logic gates are used for, to implement binary logic.

35 U.S.C. 103(a) rejection of claim 10.

Hsiao and Horiguchi, substantially teaches the claimed invention described in claims 1-9 (as rejected above).

However Hsiao and Horiguchi do not explicitly teach the specific use of a multi-bit signal embodiment for the single error signal in Figure 1 of Hsiao.

The Examiner asserts that using a multi-bit signal embodiment for the single error signal is encompassed by the Hsiao patent as an obvious engineering design choice based on circuit design requirements.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hsiao and Horiguchi by including use of a multi-bit signal embodiment for the single error signal in Figure 1 of Hsiao. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of a multi-bit signal embodiment for the single error signal in Figure 1 of Hsiao would have provided the opportunity to implement the design in the Hsiao and Horiguchi patents based on circuit design requirements.

35 U.S.C. 103(a) rejection of claim 11.

Hsiao and Horiguchi, substantially teaches the claimed invention described in claims 1-10 (as rejected above).

However Hsiao and Horiguchi do not explicitly teach the specific use of specific circuitry for implementing the binary operations required by the syndrome generators taught in the Hsiao and Horiguchi patents.

The Examiner asserts Hsiao and Horiguchi teach the use of tables to generate an intermediate error indicating value in Figure 1 from syndromes, which is mathematically equivalent to a binary matrix multiplication by a syndrome vector. It would be obvious, to use a particular set of logic gates for the error locators in the Hsiao and Horiguchi

patents to implement the required binary matrix multiplication used to produce intermediate error indication values based on obvious engineering design choices such as available circuitry, space requirements and operational speed requirements and since that is what binary logic gates are used for, to implement binary logic. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the teachings of Hsiao and Horiguchi by use of specific circuitry for implementing the binary operations required by the syndrome generators taught in the Hsiao and Horiguchi. This modification would have been obvious to one of ordinary skill in the art, at the time the invention was made, because one of ordinary skill in the art would have recognized that use of specific circuitry for implementing the binary operations required by the syndrome generators taught in the Hsiao and Horiguchi patents would have provided the opportunity for implementing the binary operations required by the syndrome generators taught in the Hsiao and Horiguchi patents based on obvious engineering design choices such as available circuitry, space requirements and operational speed requirements and since that is what binary logic gates are used for, to implement binary logic.

35 U.S.C. 103(a) rejection of claim 16.

Col. 4, lines 34 of Hsiao teach that only if any of the syndromes S1 to S8 is non-zero, i.e. not all the same zero state, an error signal is placed on an error line indicative of the error, hence if all the syndrome bits are at the zero state, no error is detected. Note:

Use of a one state in place of a zero state does not deviate from the scope or the intent of the teachings in the Hsiao patent since a 1 can be created from a 0 using an inverter.

35 U.S.C. 103(a) rejection of claim 17.

Horiguchi teaches the use of a ECCE control signal for use in bypassing error location generating circuit signals.

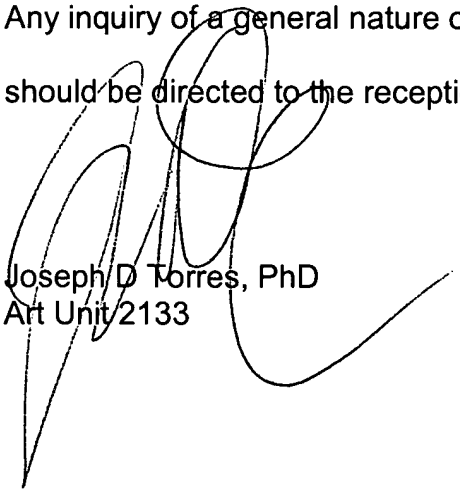
Conclusion

4. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Singh, Shanker (US 5233614 A) teaches a method of fault mapping memory while on-line.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Joseph D. Torres whose telephone number is (703) 308-7066. The examiner can normally be reached on M-F 8-5.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (703) 305-9595. The fax phone number for the organization where this application or proceeding is assigned is (703) 746-7239.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)-746-7240.



Joseph D Torres, PhD
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